HIGH-VOLTAGE VERTICAL TRANSISTOR WITH A MULTI-GRADIENT DRAIN DOPING PROFILE

RELATED APPLICATIONS

This is a continuation of application Ser. No. 11/699,936 filed Jan. 30, 2007, now U.S. Pat. No. 7,335,944, which is a division of application Ser. No. 11/042,665 filed Jan. 25, 2005, now U.S. Pat. No. 7,221,011, which is a continuation-in-part (CIP) application of application Ser. No. 10/393,759 filed Mar. 21, 2003, now U.S. Pat. No. 6,882,005, which is a continuation of Ser. No. 09/948,930 filed Sep. 7, 2001, now U.S. Pat. No. 6,573,558, all of which are assigned to the assignee of the present CIP application.

FIELD OF THE INVENTION

The present invention relates to semiconductor devices fabricated in a silicon substrate. More specifically, the present invention relates to field-effect semiconductor transistor structures capable of withstanding high voltages.

BACKGROUND OF THE INVENTION

High-voltage, field-effect transistors (HVFETs) are well known in the semiconductor arts. Most often, HVFETs comprise a device structure that includes an extended drain region that supports the applied high-voltage when the device is in the "off" state. HVFETs of this type are commonly used in power conversion applications such as AC/DC converters for offline power supplies, motor controls, and so on. These devices can be switched at high voltages and achieve a high blocking voltage in the off state while minimizing the resistance to current flow in the "on" state. The blocking or breakdown voltage is generally denoted as Vbd. The acronym Rsp refers to the product of the resistance and surface area, and is generally used to describe the on-state performance of the device. An example of a prior art HVFET having an extended drain region with a top layer of a conductivity type opposite that of the extended drain region is found in U.S. Pat. No. 4,811,075.

In a conventional HVFET the extended drain region is usually lightly doped to support high voltages applied to the drain when the device is off. The length of the extended drain region is also increased to spread the electric field over a larger area so the device can sustain higher voltages. However, when the device is on (i.e., conducting) current flows through the extended drain region. The combined decrease in doping and increase in length of the extended drain region therefore have the deleterious effect on the on-state performance of the device, as both cause an increase in on-state resistance. In other words, conventional high-voltage FET designs are characterized by a trade-off between Vbd and Rsp.

To provide a quantitative example, a typical prior art vertical HVFET (NMOS-type) may have a Vbd of 600V with a Rsp of about 16 ohm-mm^2. Increasing the length of the extended drain would affect device performance by increasing Vbd beyond 600V at the expense of a higher Rsp value. Conversely, reducing the length of the extended drain would improve the on-state resistance to a value below 16 ohm-mm^2, but such a change in the device structure would also cause Vbd to be reduced to less than 600V.

A device structure for supporting higher Vbd voltages with a low Rsp value is disclosed in U.S. Pat. Nos. 4,754,310,5, 438,215, and also in the article entitled, " Theory of Semiconductor Superjunction Devices " by T. Fujihira, Jpn. J. Appl. Phys., Vol. 36, pp. 6254-6262, Oct. 1977. In this device structure the extended drain region comprises alternating layers of semiconductor material having opposite conductivity types, e.g., PNPNP . . . . As high voltage is applied to the layers of one conductivity type, all of the layers are mutually depleted of charge carriers. This permits a high Vbd at much higher conducting layer doping concentrations as compared to single layer devices. The higher doping concentrations, of course, advantageously lower the Rsp of the transistor device. For example, in the article entitled, "A new generation of high voltage MOSFETs breaks the limit line of silicon" by G. Deboy et al., IEDM tech. Digest, pp. 683-685,1998, the authors report a vertical NMOS device with a Vbd of 600V and a Rsp of about 4 ohm-mm^2.

Another approach to the problem of achieving high-voltage capability is disclosed in the paper, " Realization of High Breakdown Voltage in Thin SOI Devices" by S. Merchant et al., Proc. Intl. Symp. on Power Devices and ICs, pp. 31-35, 1991. This paper teaches an extended drain region that comprises a thin layer of silicon situated on top of a buried oxide layer disposed on top of a semiconductor substrate. In operation, the underlying silicon substrate depletes charge from the thin silicon layer at high voltages. The authors claim that high values of Vbd are obtained as long as the top silicon layer is sufficiently thin, the buried oxide layer is sufficiently thick and the drift region doping concentration increases linearly from source to the drain. For instance, a lateral NMOS device with Vbd of 600V and Rsp of about 8 ohm-mm^2 is obtained using this approach. The same authors have disclosed their technique of manufacturing the device with linearly graded doping concentration in U.S. Pat. No. 5,300,448. Similar approaches are taught in U.S. Pat. Nos. 5,246,870, 5,412,241, 5,648,671, and 6,767,547.

Many conventional high-voltage transistors are designed to optimize breakdown voltage in the off-state. In the off-state, avalanche breakdown in high-voltage field-effect transistors typically occurs at the drain voltage at which the impact ionization integral (I) equals unity and the multiplication factor (M), defined as M=1/(1−I), approaches infinity. In the on-state, electron current flows through the drift region of the device. At high drain voltages, the electrons pass through regions of high electric field, causing impact ionization, which generates hole current in the device. If the hole current reaches a sufficiently high level, a parasitic bipolar transistor might become activated, leading to destructive breakdown of the device.

To maintain a high breakdown voltage in the on-state, the multiplication factor needs to be kept at a low level. This constraint places a limit on the maximum electric field for which the device can be designed, which limit may be less than optimal for high off-state breakdown voltage. Consequently, one problem in prior art high-voltage transistors is that the device suffers from low on-state breakdown voltage when the electric field is increased, and low off-state breakdown voltage (for a given drift length) if the field is reduced.

Although many of the device structures described above achieve high Vbd with relatively low on-state resistance as compared to earlier designs, there is still an unsatisfied need for a high-voltage transistor structure that optimizes both the on-state and off-state breakdown voltages of the device simultaneously.